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tasks)We have implemented an architectural **simulator** that uses an **IPC** specification to indicate the
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cache misses are not explicitly modeled in the **simulator**. The PI4 model has two fixed-point units
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(**IPC**)threads, and virtual memory. HigherThe **simulator** consumes user and system traces while they
using the parameters shown in Table 2-1. munication (**IPC**)threads, and virtual memory. HigherThe **simulator**
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workloads to drive a highlydetailed trace-driven **simulator** for an 8-context, 8-wide simultaneous
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the authors use a trace-driven power-performance **simulator** (based on the model by Cai [7]to report
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are generated by an execution-driven performance **simulator** [2]The **simulator** uses a cycle-accurate
This design is able to achieve 8.6% to 20% **IPC** improvements on the SPEC benchmarks. Additionally,
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For example, a generic microprocessor **simulator** can be first specialized with respect to a
was used by Volanschi to optimize the Chorus **IPC** [34]1.4 This paper In this paper, we study how
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and (2) integrated our SMT Alpha instruction set **simulator** into the SimOS **simulator** to provide an
the workload? In particular, we wish to verify the **IPC** results of previous studies to see whether they
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of these functions calls the branch predictor **simulator** to generate the branch prediction and to update
the branch penalty is defined as C *1-p) r ***ipc**)where C denotes the number of cycles wasted due
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development of commercial workloads for timing **simulators**. We describe how we address these challenges in

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and use on both NUMAchine and a complete machine **simulator**, SimOS. ii A N D O T O R Preface Like most
design, the process management design, and the **IPC** design. I was also responsible for most of the
In addition, Tornado includes a new **interprocess communication** facility, called the Protected
www.eecg.toronto.edu/~ben/thesis.ps.gz

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on Toronto's NUMAchine hardware and on the SimOS **simulator**. 1 Introduction Traditional multiprocessor
that preserves the locality and concurrency of **IPC**'s, and (iii) a new locking strategy that allows
has been handed to the cleanup system. 6 **Interprocess communication** In a microkernel system like
Tornado
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disabled. 2 Experimental Methodology The **simulator** used in this study is derived from the SIM-
2.5 3.5 x 10 0.5 1.5 2.5 3.5 Figure 1: Variation in **IPC** over time for the hydro2d benchmark. Previous
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that last on the or- Cycle-Level Performance **Simulator** Parameterizable Power Models Cycle-by-Cycle
techniques by investigating the correlation between **IPC**, power dissipation, and various architectural
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for this study. Section 3 describes the **simulator** and architecture model used. Section 4
coursé of execution correlating the behavior between **IPC**, branch prediction, value prediction, address
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main cache. In this study we use a cycle-level **simulator** of an 8-issue, speculative, out-of-order
than other traditional cache improvement schemes. **IPC** improvements of over 4% are seen for some
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the authors use a trace-driven power-performance **simulator** (based on the model by Cai [5]to report
or the power [8] without significantly impacting the **IPC** (instruction per cycle) performance. In [6]the
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Confidence Estimation for Branch Prediction Reversal - Aragón, González, García.. (2001) (Correct)
(2 citations)
using a modified version of the sim-safe **simulator** [2]The number of branch hits and misses of a
rate, as well as its performance in terms of **IPC**. Finally, Section 5 summarizes the conclusions of
www.ditec.um.es/~jlaragon/papers/BPRU-HIPC-2001.pdf

Predictive Techniques for Aggressive Load Speculation - Glenn Reinman (1998) (Correct) (10 citations)
8. 2 Methodology and Baseline Architecture The **simulators** used in this study are derived from the
Base %ld %st Program Input exec (M) fastfwd (M) **IPC** exe exe compress ref 93 0 1.93 26.7 9.5 gcc
www-cse.ucsd.edu/users/calder/papers/MICRO-98-LoadSpec.ps

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(19 citations)
4-way in-order issue superscalar processor **simulator** with a 16k directmapped non-blocking data

Per Cycle Figure 2: Impact of Load Latency on **IPC**. calculation. If the address is mispredicted, the
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